TITLE: Method and arrangement for implementing intra-frame interleaving

TECHNOLOGICAL FIELD

The invention concerns generally the technology of interleaving transmission symbols in a radio transceiver in time domain. Especially the invention concerns the technology of implementing intra-frame interleaving in multicode transceivers of the proposed UTRA (Universal Terrestrial Radio Access) system.

BACKGROUND OF THE INVENTION

The Layer 1 multiplexing and channel coding characteristics of the FDD (Frequency Division Duplex) mode of the UTRA are, at the priority date of this patent application, defined in the document "TS 25.212 V3.0.0 (1999-10), 3rd Generation Partnership Project (3GPP); Technical Specification Group (TSG) Radio Access Network (RAN); Working Group 1 (WG1); Multiplexing and channel coding (FDD)" available through the 3GPP. Fig. 1 illustrates the transport channel multiplexing structure for uplink as defined in said document. The functional blocks the serial connection of which is shown in the upper part of Fig. 1 are CRC attachment 101, transport block concatenation and code block segmentation 102, channel coding 103, radio frame equalisation 104, first interleaving 105, radio frame segmentation 106 and rate matching 107. Several entities of the above-described kind may be coupled to the inputs of a transport channel multiplexing stage 108, the output of which is further coupled to the serial connection of physical channel segmentation 109, second interleaving 110 and physical channel mapping 111.

In the downlink direction there may be certain modifications to the arrangement of functional blocks shown in Fig. 1, but at least the lower end of the arrangement which consists of the physical channel segmentation, second interleaving and physical channel mapping entities remains the same. For the purposes of the present invention it suffices to analyze the operation of the second interleaving and physical channel mapping blocks.

The aim of the second interleaving 110 is to permutate the bits in time domain so that bits that originally were close to each other in the bit stream to be transmitted are separated from each other in the time domain for the duration of their travel over

the radio interface. This way a short interval of extremely bad interference conditions at the radio interface should not cause any bursts of several consecutive erroneous bits in the received and decoded bit stream. The second interleaving 110 takes place in inter-frame manner meaning that the data entity subjected to interleaving is one radio frame.

Fig. 2 illustrates the operation of the second interleaving stage. The bits that come as an input stream 201 to the interleaver are written into a bit array 202 which has a certain number of rows and a certain number of columns. The numbers shown in the input stream and the bit array are simply the serial numbers of the bits in the radio frame. Here the number of columns is shown to be 32, with column numbers ranging from 0 to 31. The columns are fed into an intercolumn permutator 203 which rearranges them into a different order. As examples, the 0th column remains 0th, the 17th column comes 1st, the 14th column comes 30th and the 31th column remains 31th after the intercolumn permutator 203. The bits are read from the permutated columns to the output of the second interleaving stage column by column. The bit stream 204 with the serial number of certain bits is shown as the output of the second interleaving stage.

The TDD or Time Division Duplex mode with its possibility of simultaneously using several spreading codes brings about some complications to the presented arrangement. If a single spreading code is used to transmit the bit stream, the bit stream 204 is transmitted by using that spreading code. However, in a multicode situation the transmitting device has at least two spreading codes at its disposal, and it transmits by using these parallel spreading codes simultaneously during a single time slot. The presently defined physical channel mapping arrangement is such that the parallel spreading codes are filled one at a time with bits taken from the bit stream 204. This may lead to the situation shown at the bottom of Fig. 2 where, during a certain time slot, e.g. bits 0 and 14, bits 32 and 46 and so on of a certain frame are transmitted simultaneously. Currently the number of parallel spreading codes may vary between 2 and 9.

The arrangement according to Fig. 2 has the drawback of in the multicode situation canceling much of the advantages usually obtained through the second interleaving, because certain bits that are near to each other in the frame are practically not separated at all in the time domain at the radio interface. The nature of the interference occurring in UTRA systems is such that it may occur e.g. that a part of a time slot either from the very beginning or from the very end of the time slot gets

erased due to interference, especially inter-operator interference. The result of such an erasure, taken the arrangement of Fig. 2, is a burst of errors very close to each other in a received frame.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method and an arrangement for ensuring that the separation in time between adjacent bits in a frame does not suffer in a multicode transmission arrangement. It is a further object of the invention that major changes in the existing proposed arrangements could be avoided.

The objects of the invention are achived by modifying the order in which the bits are mapped into the spreading codes after the second interleaving stage.

The method according to the invention is meant for interleaving a stream of data consisting of digital information symbols prior to transmission over a radio interface. It comprises the steps of
- performing a permutation to the stream of digital data, thus producing a permutated stream of digital data,
- producing, from the permutated stream of digital data, at least two component streams
- mapping each component stream into a spreading code.

It is characterized in that it comprises the step of reversing the order of information symbols in at least one component stream prior to mapping it into a spreading code.

The invention also applies to a transmitter arrangement which comprises
- means for performing a permutation to the stream of digital data, thus producing a permutated stream of digital data,
- means for producing, from the permutated stream of digital data, at least two component streams
- means for mapping each component stream into a spreading code.

It is characteristic to the radio device that it comprises means for reversing the order of information symbols in at least one component stream prior to mapping it into a spreading code.

The present invention is based on a finding that the mapping of bits into the parallel spreading codes has a key role in maintaining the separation of bits in the time

domain. An advantageous way to eliminate the drawbacks of the existing arrangements is to modify the order in which the bits are mapped at least to a part of the spreading codes.

In order not to cause major changes into the existing proposed arrangement it was found that if in every second one of the component bit streams that are parts of the output of the second interleaver the order of bits is inverted, sufficient separation in time domain between bits is maintained. Such a modification contains essentially no added complexity, because the order in which a certain finite bit stream is read (from first bit to last bit or from last bit to first bit) is merely a question of choosing a certain memory access command properly.

The invention requires only a minor change in the existing proposed arrangements, and yet it provides a significant relief to the problem of maintaining sufficient separation in time domain between bits that are close to each other in the frame.

BRIEF DESCRIPTION OF DRAWINGS

The novel features which are considered as characteristic of the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Fig. 1 illustrates a known transport channel multiplexing structure for uplink,

Fig. 2 illustrates the results of second interleaving and code mapping in the arrangement of Fig. 1,

Fig. 3 illustrates the results of second interleaving and code mapping according to an advantageous embodiment of the invention,

Fig. 4 is a flow diagram of the method according to the invention and

Fig. 5 illustrates a radio device according to an embodiment of the invention.

Figs. 1 and 2 were already accounted for in the description of prior art. Like parts in the drawings are shown with the same reference designators.

DETAILED DESCRIPTION OF THE INVENTION

The upper part of Fig. 3 is similar to that of Fig. 2: The bits that come as an input stream 201 to a second interleaver are written into a bit array 202 which has a certain number of rows and a certain number of columns. Here the number of columns is again 32, with column numbers ranging from 0 to 31. The columns are fed into an intercolumn permutator 203 which rearranges them into a different order. The present invention does not change the operation of the intercolumn permutator, so the 0th column remains 0th, the 17th column comes 1st, the 14th column comes 30th and the 31th column remains 31th after the intercolumn permutator 203 just as in the prior art arrangement of Fig. 2.

The invention pertains to the order in which the bits are read from the permutated columns to the output of the second interleaving stage, which is also the input of the physical channel mapping stage. The bit stream 204 with the serial number of certain bits is shown as the known output form of the second interleaving stage. However, when the bits are mapped therefrom to the parallel spreading codes of which there are two in Fig. 3, the order of bits in the component bit stream that goes into the second spreading code is reversed.

The principle shown in Fig. 3 is easily generalized to the case of N parallel spreading codes, where N is a positive integer greater than 2, by stating that the bit order in every second component bit stream is reversed before mapping that component bit stream into the corresponding spreading code.

The invention does not limit the choice of the actual physical step in which the inverting of bit order is made for every second component bit stream. The system specifications of communications systems like the UTRA do not usually specify any particular hardware implementation for performing the standardized operations, but these are left into the discretion of transceiver designers. One advantageous way to perform the reversing is to integrate it into the step in which the bits are read from the bit array 202 after column permutation: the step of permutating columns does not mean anything else than correctly selecting the order in which bits are read from the memory locations where they are stored when they are said to be in the bit array.

The transceiver may reorganize this reading order that in addition to the permutated order of columns, it takes into account the fact that those columns that go to the bit streams destined to be reversed are read in an inverted order and from bottom to top in the array representation.

Fig. 4 illustrates a method according to an advantageous embodiment of the invention in the form of a flow diagram. The steps shown in Fig. 4 belong functionally to the second interleaving stage 110 shown in Fig. 1. Step 401 corresponds to writing the input bits into a bit array, and step 402 corresponds to permutating the columns. At step 403 the transceiver checks the number of spreading codes it has at its disposal for transmitting this particular frame. If the number of codes is only one, the permutated columns are output in the known order so that they can be correctly mapped into the spreading code at step 406. If, however, there is a positive finding at step 403, component streams are (at least conceptually) composed at step 404 and in every second one of these the bit order is reversed at step 405.

Fig. 5 illustrates the structure of a mobile terminal or base station where the parts from the CRC attacher 101 to the physical channel segmentator 109 may be similar as in known devices that conform to the TS 25.212 document mentioned in the description of prior art. The second interleaver 510 and the physical channel mapper 511 together are arranged to implement the method illustrated in Fig. 4; the physical implementation of the method is straightforward and within the capabilities of a person skilled in the art on the basis of the above-given instructions.

The above-given exemplary embodiments should not be construed as limiting the applicability of the invention; the latter is merely reflected in the scope of the appended claims. For example the invention does not require that an interleaving operation where every second component stream to be mapped into a spreading code should be limited to interleaving within a single time slot. Similarly the permutation and order inverting operations may be performed on groups of bits (e.g. so that three consecutive bits constitute a group) instead of just bits.